Schedule For Faculty Development Programme on "Digital VLSI " at IIT Guwahati

DAY-1 Introduction to VLSI and Digital Design

09:00 AM – 09:30 AM	**On-Spot Registration**
09:30 AM - 11:00 AM	Introduction to VLSI Design by **Dr. Gaurav Trivedi (Assistant Prof. EEE Department IIT Guwahati)**
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 1:15 PM	Introduction to VLSI Design by **Dr. Gaurav Trivedi (Assistant Prof. EEE Department IIT Guwahati)**
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Introduction to Digital Design and Comp Architecture by **Dr. John Jose (Assistant Prof. CSE Department IIT Guwahati)**
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	Introduction to Digital Design and Comp Architecture by **Dr. John Jose (Assistant Prof. CSE Department IIT Guwahati)**

DAY-2 FPGA design flow using Vivado

09:00 AM	**Reporting Time**
09:00 AM - 10:00 AM	7-Series Architecture Overview
10:00 AM - 11:00 AM	**Lab 1:** Vivado Design Flow
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 12:15 PM	Synthesis Technique
12:15 PM – 1:15 PM	**Lab 2:** Synthesize a design with the default settings as well as other settings changed and observe the effect
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 3:** Implement the synthesized design of previous lab, generate bitstream, download the bitstream and verify the functionality.
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 3: Session Continue**

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DAY-3 FPGA design flow using Vivado

09:00 AM	**Reporting Time**
09:00 AM - 11:00 AM	Introduction to IP Integrator
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 01:15 PM	**Lab 4:** Using the IP Catalog and IP Integrator • Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab5:** Xilinx Design Constraints • Create a project with I/O Planning type, enter pin locations, and export it to the RTL Pre & Post synthesis analysis
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 5:** Session Continue.

DAY-4 Clocking resources implementation in vivado & static timing analysis

09:00 AM	**Reporting Time**
9:00 AM - 11:00 AM	Introduction to **static timing analysis** • Implementation and static timing analysis with examples
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 1:15 PM	**Lab 6:** Simple Hardware Design using MMCM • Create a Vivado project and use IP Integrator instantiation of MMCM & its features • Explanation of different timing paths & create the timing constraints and perform the timing analysis.
01:15 PM – 02:00 PM	**Lunch Break**
02:00 AM - 04:00 AM	Lab 7: Hardware design using PLL • Extend the hardware system by adding PLL with example verilog coding • Synchronous & Asynchronous circuits

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DAY-4 Clocking resources implementation in vivado & static timing analysis

04:00 PM - 04:15 PM	Tea Break
04:15 PM - 06:00 PM	**Lab 8: FSM design** • Coding in Verilog and explaining advantages and disadvantages of clocking resources on the design • Checking/ correcting timing errors

DAY-5 Block Memory implementation in vivado

09:00 AM	**Reporting Time**
09:00 AM - 10:00 AM	Introduction to block memory
10:00 AM – 11:00 AM	**Lab 9: Simple Hardware Design using block memory** • Create a Vivado project and use IP Integrator instantiation of block memory& its features
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 1:15 PM	**Lab 10**: Designing FIFO • Extend the hardware system by adding FIFO with example verilog coding
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 11: Creating simple UART** • Adding FIFO in UART coding in Verilog and explaining advantages and disadvantes of FIFO/block memory on the design
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 11** : Session Continue.

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DAY-6 FSM implementation in Vivado & XSIM simulation

09:00 AM	Reporting Time
9:00 AM - 11:00 AM	Introduction to various FSM design
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 1:15 PM	**Lab 12: Simple pattern detector using FSM** • Create a Vivado project and simulate Pattern detector by writing testbenches
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 13: Testbenches features & Vivado simulation features** • Mealy & Moore FSM simulation
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 14: Creating simple UART** • UART coding in Verilog and explaining simulation of it

DAY-7 Vivado logic analyzer & its features

09:00 AM	Reporting Time
9:00 AM - 11:00 AM	Hardware implementation and Vivado logic analyzer
11:00 AM - 11:15 AM	Tea Break
11:15 AM – 1:15 PM	**Lab 15: Implemeting pattern detector in hardware and debugging using vivado logic analyzer** • Create a Vivado project and bit file generation with vivado logic analyzer netlist debugging on hardware
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 16: Teraterm/hyperterminal based testing with vivado logic analyzer** • Real time testing of UART – explaining the features of Vivado logic analyzer •Use Mark Debug feature and also available Integrated Logic Analyzer(ILA) core (available in IP Catalog) to debug the hardware.
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 16: session continue & Power Analysis**

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DAY-8 Introduction to HLS

09:00 AM	Reporting Time
09:00 AM - 11:00 AM	Introduction to HLS
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	**Lab 17: Creating Project and Understanding Reports** Experience a basic design flow of Vivado HLS and review generated output. Improving Performance
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 18: Optimizing Performance through Pipelining** • Use pipelining technique to improve performance & Data Types
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 18: Session Continue**

DAY-9 Optimizing Techniques

09:00 AM	Reporting Time
09:00 AM - 11:00 AM	Optimizing for Area and Resources
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	**Lab 19: Improving Area and Resource Utilization** Use directives to optimize resource sharing. Handling Block- and Port-Level Protocols Coding Considerations Creating a Processor System
01:00 PM – 02:00 PM	Lunch Break
02:00 PM – 04:00 PM	**Lab 20: Designing an Audio System** • Use IP-XACT export capability of Vivado HLS to generate an IP and integrate the generated core in an embedded system developed using IP Integrator.
04:00 PM – 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 20 : Session Continue**

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DAY-10 Embedded System Design Using FPGA

09:00 AM	**Reporting Time**
09:00 AM - 11:00 AM	Introduction to Embedded System Design using Zynq-7000 SOC
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	**Lab 21: Simple Hardware Design** Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board. Zynq Architecture, Extending the Embedded System into Programmable Logic
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	**Lab 22: Adding Peripherals in Programmable Logic** • Extend the hardware system by adding AXI peripherals from the IP catalog. • Adding Your Own IP Peripheral
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	**Lab 23: Creating and Adding Your Own Custom IP** • Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral.

DAY-11 Digital Design concepts using SCL PD cases with Hands-on.

09:00 AM - 11:00 AM	Digital Design concepts using SCL PD cases with Hands-on.
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	Session continue
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Session Continue
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	Session Continue

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DAY-12 Digital Design concepts using SCL PD cases with Hands-on.

09:00 AM - 11:00 AM	Digital Design concepts using SCL PD cases with Hands-on.
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	Session continue
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Session Continue
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	Session Continue

DAY-13 Digital Design concepts using SCL PD cases with Hands-on.

09:00 AM - 11:00 AM	Digital Design concepts using SCL PD cases with Hands-on.
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	Session continue
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Session Continue
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	Session Continue

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DAY-14 Digital Design concepts using SCL PD cases with Hands-on.

09:00 AM - 11:00 AM	Digital Design concepts using SCL PD cases with Hands-on.
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	Session continue
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Session Continue
04:00 PM - 04:15 PM	Tea Break
04:15 PM – 06:00 PM	Session Continue

DAY-15 Digital Design concepts using SCL PD cases with Hands-on.

09:00 AM - 11:00 AM	Digital Design concepts using SCL PD cases with Hands-on.
11:00 AM - 11:15 AM	Tea Break
11:15 AM - 1:15 PM	Session continue
01:15 PM – 02:00 PM	**Lunch Break**
02:00 PM - 04:00 PM	Certificate Distribution
04:00 PM - 04:15 PM	Tea Break