

## Registration

Name of the Applicant (first, last):  
.....  
Fathers Name.....  
Gender: .....  
Designation: .....  
Highest Qualification: .....  
Name and Address of the Organization/Institute:.....  
.....  
Category : (GEN/OBC/SC/ST/Others).....  
City/town:.....  
Email:.....  
DOB:.....  
Mobile Number:.....  
Do you need accommodation?  
(Yes/No):.....  
Transaction ID (Applicable for Online  
Transaction):.....  
Signature of the Applicant:.....  
Signature and Seal of the Forwarding Authority  
Name .....  
Designation .....

Affix passport  
size  
photograph

Note: The Faculty/Staff are requested to submit the NOC from respective department before attending the session.. Caste certificate in case of SC/ST/OBC. For accommodation please contact(+91-8876634585)

## Registration Fee including GST

### Registration Fee

(Including Course Material, Snacks and Lunch )

Rs. 2,950/- for Faculty, Lab Technicians and Project Staff

Rs. 1,475/- for SC/ST Faculty

Rs. 5,900/- for Industry Personnel, Research Scholars and Students.

**Mode of Payment: Online Only  
(RTGS/NEFT)**

### For Online Transfer

**Bank Name: State Bank of India**

**Account Name: IIT Guwahati R&D E&ICT Academy**

**Account No.: 36071160089**

**IFSC Code: SBIN0014262**

**Bank Name: State Bank of India**

**Bank Address: IIT Guwahati, GHY- 39.**

## Course Coordinators from Academy

- **Prof. Ratnajit Bhattacharjee**  
Principal Investigator  
E&ICT Academy, IIT Guwahati
- **Dr. Gaurav Trivedi**  
Co-Principal Investigator  
E&ICT Academy, IIT Guwahati

## Course Coordinators from NIT Mizoram

- **Dr. Chaitali Koley**  
Assistant Professor (HoD)  
ECE Dept, NIT Mizoram
- **Mr. Sushanta Bordoloi**  
Trainee Teacher  
ECE Dept, NIT Mizoram

## Expert from Industry

- **Mr. H.Balachander**  
FAE Manager CoreEL Technologies

## How To Reach NIT Mizoram

### By Air:

Aizawl can be reached by Air through Kolkata / Guwahati. The NIT Mizoram is approximately 35 Km far from Lengpui (Aizawl) Airport. Pre-paid Taxis are easily available from the Airport to reach the Institute. The taxi fare is Rs 700 to 800.

### By Train:

Silchar is the nearest railway station to Aizawl. The journey (by road) from Silchar to Aizawl may take approx. 6 Hrs. Sumos (share basis) are available from Mizoram Circuit House, Sonai Road, Silchar.

### By Bus / Sumo:

Guwahati to Aizawl: Private Buses (Network, Capital, etc.) are available from Guwahati. Booking Counters for these buses are located at Paltan Bazar. Bus usually leaves at 02:00 PM. The journey to Aizawl by Bus is approx. 24Hrs. Sumos are available from Mizoram House, Christian Basti G S Road, Guwahati (Evening). The journey to Aizawl by sumo is approx. 20 Hrs. Silchar to Aizawl: Sumos are available from Mizoram Circuit House, Sonai Road, Silchar. The sumo fare is Rs 300.

Inner Line Pass (ILP) is required for entry into Mizoram and can be obtained from Liaison Officer, Government of Mizoram from the following cities Kolkata, Silchar, Shillong, Guwahati or New Delhi. Airport has its own mechanism to facilitate ILP application on arrival. For detail visit : <http://mizoram.nic.in/more/ilp.htm>



सत्यमेव जयते

An Initiative of Ministry of Electronics &  
Information Technology (MeitY)

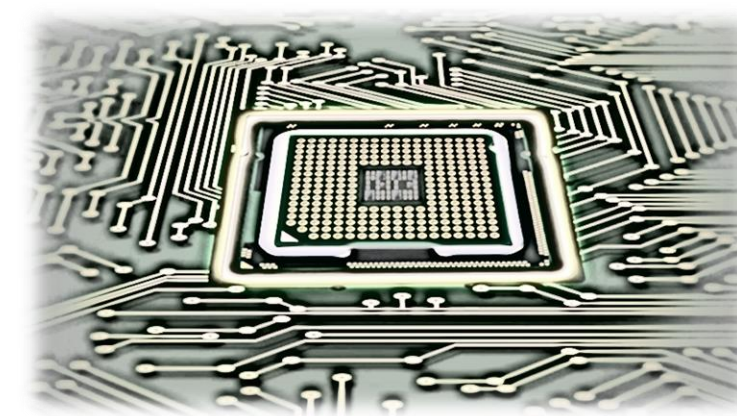
Government of India.

Electronics & ICT Academy  
IIT Guwahati, Assam

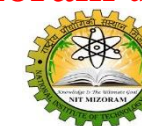


Faculty Development Programme on

VLSI Design using FPGA Tools



Organized in association with  
**NIT Mizoram** under TEQIP -III



&

Support from  
**CoreEL Technologies**

CoreEL  
Technologies

Course Date:05-11 March, 2018

Last Date of Registration: 01.03.2018

(Online Registration Link will be open from 01.02.2018)

Venue: NIT Mizoram

## Course Outcome

The participants are expected to understand:

- Understand FPGA specific coding guidelines in RTL Design
- Compare the RTL for simulation and synthesis in FPGA design flow
- Synthesize the design as per the specification
- Recognize the synthesis and simulation mismatches in RTL Design and its relevance in FPGA design environment
- Use IP cores in FPGA based system design
- Perform timing analysis and interpret timing reports in FPGA based designs
- Illustrate the steps involved in FPGA design implementation
- Work on hardware debugging in FPGA's
- Explain the need for FPGA's in SoC applications

## Assignments and Project

Assignments will be of the following type:

- Lecture sessions
- Instructor led hands-on sessions with 30% lecture and 70% hands on a daily basis
- MCQ model reviews for each topic
- Assignments and Projects

## Preferred Pre- Requisites for the Course

The preferred pre-requisites for the course are:

- Basic Digital Concepts.
- Basic Knowledge on Verilog.

## Hands-on Topics

Lab sessions

- Lab session - Design entry and simulation of given design
- Exercises on STA concepts
- Assignments on modeling of digital blocks

**For details of the programme and course contents etc., please log on to Electronics and ICT Academy website:**  
<http://eict.iitg.ernet.in/>

## Topics Covered

Following topics will be covered during session :

- Digital System Design using Verilog.
- Lab session - Design entry and simulation of given design
- Logic Synthesis
- Synthesizable HDL and coding guidelines
- Basics of Timing Analysis
- Exercises on STA concepts
- Interpreting timing reports
- Embedded System Design using FPGA's
- Zynq FPGA architecture & design flow
- Assignments on Modeling of digital blocks.
- Logic Synthesis of the given design using Vivado and results analysis.
- Exercises on STA concepts.

## About NIT Mizoram

The Ministry of Human Resources Development, Govt. of India vide its order no. F. 23-13-2009-TS-III Dated 30th of Oct. 2009 and 3rd March 2010, had decided to set up ten new NITs. In view of the above NIT Mizoram was started in the year 2010 in the state of Mizoram with an objective to impart education, research & training leading to B.Tech, M.Tech & PhD. degrees. This institute has been declared as an Institute of National Importance by an Act of Parliament. Here the students are admitted through All India Entrance Exam- Joint Entrance Exam (JEE Main) & CCMT.

## About E&ICT IIT Guwahati

Electronics and ICT Academy is an initiative of Ministry of Electronics & Information Technology (MeitY), Govt. of India for Faculty/ Research Scholar Development Programme.

Academy has planned short term training programmes on fundamental and advanced topics in IT, Electronics & Communication, Product Design, Manufacturing with hands on training and project work using latest software tools and systems.

In addition, the Academy will conduct specialized/customized training programmes and research promotion workshops for corporate sector & educational institutions.

## Objective of the Course

Course Objective is to provide basic knowledge in Digital VLSI using FPGA board. The programme will focus on practical aspects and include examples which are relevant to the current industry requirements.

Lab sessions will include the following:

- FPGA design flow using Vivado.
- Digital system design using verilog.
- RTL simulation concepts.
- Implementing Digital Designs on FPGA board using Vivado.
- Clocking resources implementation in Vivado & Static timing analysis.
- Implementing timing analysis using Vivado.
- FSM implementation in Vivado & XSIM simulation
- SOC Designing

## Who Can Attend

Programme is open to Faculty Members, Research Scholars, PG & UG Students, Lab Technicians and Project Staffs from Universities, Colleges & Schools. Industry Personnel working in the concerned/allied discipline may also apply.

## How to Apply

**Online** – The participants may log on to the E&ICT Academy, IIT Guwahati website: <http://eictacad@iitg.ernet.in> and fill up the google doc application form.

## Contact Details

**For more details or any queries please contact  
Program Manager, E&ICT Academy IIT  
Guwahati**

**Email:** [eictacad@iitg.ernet.in](mailto:eictacad@iitg.ernet.in),  
[eictacad@gmail.com](mailto:eictacad@gmail.com)

**Phone No:** +91-36125863182/3009